ATMEL WHITE PAPER

Single Cycle 8051 Core – AT89LP Family of High Performance & Low Power Flash Microcontrollers

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Summary

The AT89LP family of products features a single-cycle 8051 core within a highly integrated microcontroller allowing designers to achieve 6x to 12x more performance compared to classic 8051 devices. The 8051 architecture has been used in the industry for decades and remains very popular with system developers. AT89LP microcontrollers offer full binary code compatibility with the original MSC®51 instruction set, ensuring an easy migration path. The single-cycle core provides designers a unique opportunity to upgrade their application with more performance (up to 20 MIPS), less power consumption (up to 80% savings) and code size ranging from 2KB to 256KB. AT89LP microcontrollers reduce system cost and enable faster time-to-market by integrating more system features on chip.

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Introduction

Atmel® introduced the first 8-bit Flash microcontroller in 1993. This first-generation Flash microcontroller was based on the classic 8051 core. The on-chip Flash memory retained its contents even after power was turned off, and was electrically erasable and programmable. Atmel's 8051 8-bit microcontrollers were the industry's first Flash based microcontrollers featuring In-System Programming. Atmel was again the first to develop the In-Application Programming feature in its Flash microcontrollers thereby enabling remote upgrades.

Single-Cycle AT89LP Family

The Atmel AT89LP family is based on a low power, high performance 8-bit Single-Cycle 8051 Core. The classic 8051 CPU requires 12 clock cycles for every byte fetch, whereas the new AT89LP CPU requires only one clock cycle for every byte fetch. The AT89LP family instructions need only 1 to 4 clock cycles to complete, thereby providing 12 times or higher throughput than the classic 8051. Seventy percent of the instructions execute in the same number of clock cycles as the number of bytes to be fetched. The AT89LP Core is capable of 20 MIPS (Millions of Instructions Per Second) throughput at 20 MHz clock frequency. In comparison, the classic 8051 architecture delivers less than 2 MIPS at 20 MHz. Conversely, at the same MIPS throughput as the classic 8051, the new AT89LP Core runs at a much lower clock frequency, thereby greatly reducing power consumption. The AT89LP devices can operate down to 2.0V supply voltage.

Typical consumptions of AT89LP devices:

- Active mode 1.1 mA @ 3.6V, 1 MHz
- Idle mode 0.43 mA @ 3.6V, 1 MHz
- Power-down mode <1 µA @ 3.6V

Reduced Power Consumption :

5.5V	**AT89LP**	**AT89**
Active Mode	1.59 mA @ 1 MHz	7.5 mA @ 12 MHz
Idle Mode	0.56 mA @ 1 MHz	1.48 mA @ 12 MHz
Power Down Mode	<2 uA	14.3 uA

Atmel's AT89LP Single-Cycle 8051 microcontrollers are optimized for low power and high performance applications. The AT89LP microcontrollers reduce system cost and enable faster time-to-market by providing such features as: In-Application Programmable Flash, On-Chip Flash data, Pulse Width Modulator, 10-bit A/D Converter, Analog Comparator, Internal Oscillator, Watchdog Timer, SPI and On-Chip-Debug.

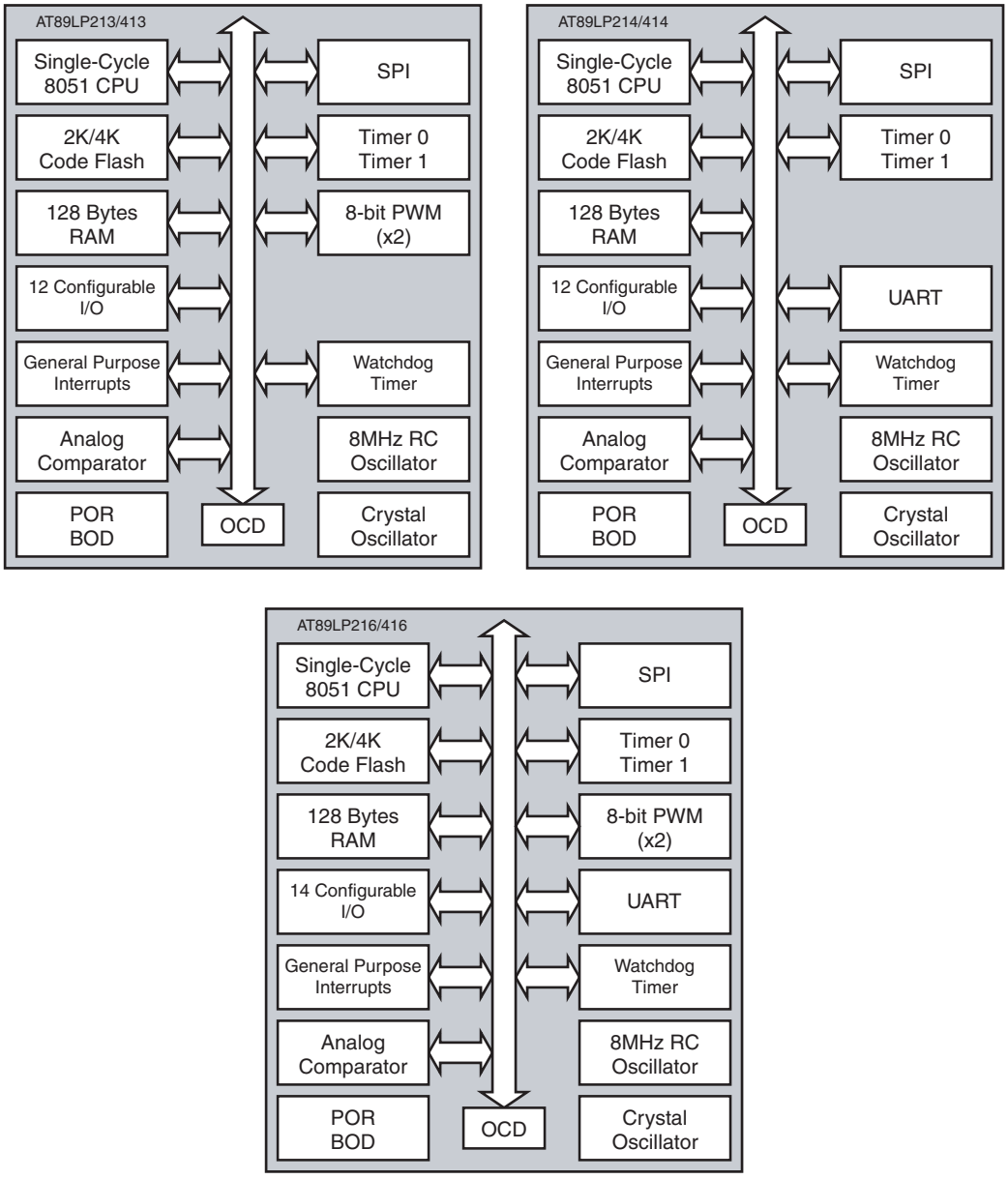
AT89LP Family Improvements

The Single-Cycle AT89LP family of devices offer enhanced features accessible through instructions that are 100% binary compatible with the traditional 8051 instruction set. The Special Function Register (SFR) addresses and bit assignments are compatible with current Atmel 8051 microcontrollers. The following key architectural improvements make the AT89LP family devices fit for low power, yet high performance applications.

- **System Clock:** The CPU clock frequency equals the XTAL1 frequency. The crystal oscillator no longer needs division by 2.
- **CPU:** The CPU fetches one byte from code memory every clock cycle instead of every twelve clock cycles. This greatly increases the throughput of the CPU and reduces the power consumption. As a consequence, the CPU no longer executes instructions in 12 to 48 clock cycles, but only in 1 to 4 clock cycles.
- **Timer/Counters:** The Timer/Counters in the AT89LP devices are enhanced in Mode 0 as a variable 9- to 16-bit timer/counter and in Mode 1 as a 16-bit auto-reload timer/counter. In the new architecture the Timer/Counters increment at a rate of once per clock cycle. This compares to once every 12 clocks in the classic 8051.
- **Serial Port:** The AT89LP UART supports Automatic Address Recognition and Frame Error Detection. Its baud rate in Mode 0 is 1/2 the clock frequency, compared to 1/12 the clock frequency in the classic 8051.
- **I/O Ports:** The I/O ports may be configured in four different modes: input-only (tristated), full CMOS output, open-drain output and quasi-bidirectional (classic 8051).
- **Reset:** The RST pin is active-low as compared with the active-high reset in the classic 8051, resulting in reduced latch-up susceptibility.

Block Diagram

Figure 1. AT89LP*xxx* Block Diagram



Key Advantages

AT89LP microcontrollers have the following key advantages:

- Binary compatibility with the industry standard MCS®51 instruction set
- Access to a wide range of existing code libraries and development tools from several vendors
- Lower power consumption and reduced EMI for the same throughput as classic 8051s
- 6x to 12x quicker interrupt response times and faster pin toggling than classic 8051s
- Fully static CMOS logic implementation driven by a single system clock
- Totally deterministic response at 20 MIPS (no cache memory)
- Boolean processor (bit set/reset read-modify-write instructions execute in two-cycles)
- Power saving modes of operation (Idle and Power-down) with multiple interrupt-based wake-up sources
- Fast programming time using Page Mode
- In-Application Programming for the added power of self-modifying code
- DSP-grade CPU speed using built-in hardware multiplier and fast dual data pointers
- Small footprints for space constrained applications
- Wide voltage operating range to meet a variety of needs
- Higher than voltage supply tolerant I/Os
- Upward migration path to devices with larger memories or more I/Os
- On-Chip Debug system allows development of firmware within the target system

System Integration

Atmel AT89LP microcontrollers are built around an enhanced 8051 CPU and are fully binary compatible with the industry standard MCS®51 instruction set. The CPU employs a simple two-stage pipeline to fetch and execute one instruction byte every clock cycle, allowing up to 1 MIPS per MHz of system frequency. The enhanced CPU is paired with on-chip RAM and a range of integrated peripherals, including at least two 16-bit timers, multi-phasic pulse width modulator (two to four phases), an enhanced UART, a master/slave SPI, debounced analog comparators, 10-bit analog-to-digital converter, watchdog timer, and pin-based configurable interrupts. The devices also include system functions such as Power-on Reset, Brown-out Detection and an on-chip high precision RC Oscillator. The devices include 2KB up to 256KB of In-System Programmable Flash memory for code storage and up to 64KB of on-chip Flash data memory. The high level of system integration on AT89LP devices provides reduced system cost, lower power consumption and faster time-to-market.

Timer/Counters

AT89LP microcontrollers have two or more 16-bit timers for use as system timers or event counters. Timer 0 and Timer 1 can independently generate 8-bit pulse width modulation waveforms. Timer 2 can be used with the Compare/Capture Array (CCA) to capture events and perform measurements on multiple channels or to generate multi-phasic PWM waveforms with 2 to 4 phases for advanced motor control.

Serial Communication

AT89LP microcontrollers include a full Serial Peripheral Interface (SPI) bus for high-speed serial communication with both master and slave modes; and an enhanced UART with automatic address recognition and framing error detection.

Analog Peripherals

AT89LP microcontrollers include one or more analog comparators with selectable interrupt modes and a tunable digital debouncer. Some devices also include an integrated 10-bit analog-to-digital converter with multiple input channels and single-ended or fully differential operation.

Configurable I/O

Each pin of an AT89LP microcontroller is independently configurable in one of four modes: input-only (high impedance), open-drain, push-pull CMOS output, or Quasi-bidirectional (Intel). Some devices tolerant voltages levels on the I/Os that are greater than the supply voltage. In addition, all pins of Port 1 may be configured to generate an interrupt for a variety of edge or level conditions.

Supervisory Functions

AT89LP microcontrollers integrate several supervisory functions on chip, including Power-on Reset, Brown-out Detection, Software Reset, and a Watchdog Timer.

Clock Selection

The AT89LP devices can be clocked from several clock sources, including:

- External clock source
- On-chip crystal oscillator in high or low frequency mode
- Internal 8 MHz RC oscillator with ±5% accuracy over the entire operating range

Power Reduction

AT89LP microcontrollers include two power-saving modes of operation: Idle and Power-down. These modes can be exited through a variety of interrupt conditions.

Example Applications

The majority of embedded applications continue to be based on 8-bit devices. AT89LP microcontrollers provide high levels of integration leading to reduced system cost, lower power consumption, smaller packages, and faster time-to-market. These devices are ideal for communications, consumer, and industrial products, ranging from battery-powered devices to white goods. Some example uses include:

- Protocol Conversion
  - Create a low-cost SPI—UART bridge.
  - Convert the parallel port of a legacy device to an SPI bus .
- Intelligent Electronics
  - Replace discrete logic components and programmable logic devices in control systems with an AT89LP device for the added flexibility of a microcontroller.
  - Create smart sensors using the integrated ADC.
  - Configure intelligent displays using the high current capability of the I/O drivers.
  - Incorporate a low-cost, small package AT89LP device into disposable electronics for medical or drug testing.
- Waveform Capture and Generation
  - Capture and process multi-channel events with the Compare/Capture Array.
  - Drive electric motors with the up to four-phasic PWM.
  - Use the on-chip timers for pulse generation, programmable frequency sources, or remote control encoders.
  - Encode speech waveforms for direct digital speaker drive.

Table 1. Applications

Communications	Consumer	Industrial
Handset Display Microphone Display Protocol Conversion Speech Encoder Telephone Handset	Disposable Electronics Handheld Devices Intelligent Displays Smoke/CO Detectors Thermostat Toys Universal Remote Control White Goods	Data Acquisition Motor Control Portable Instruments Smart Relays

Device Overview

	On-chip Memory			Timer/Counters			Serial Interfaces		Analog			
Device	CODE	DATA	RAM	16-bit	PWM	CCA	UART	SPI	COMP	ADC	Pins	Available
AT89LP213	2K		128	2	2	N	N	Y	Y	N	14	Now
AT89LP214	2K		128	2	N	N	Y	Y	Y	N	14	Now
AT89LP413	4K		128	2	2	N	N	Y	Y	N	14	Q4 2006
AT89LP414	4K		128	2	N	N	Y	Y	Y	N	14	Q4 2006
AT89LP216	2K		128	2	2	N	Y	Y	Y	N	16	Now
AT89LP416	4K		128	2	2	N	Y	Y	Y	N	16	Q4 2006
AT89LP2052	2K		256	2	2	N	Y	Y	Y	N	20	Now
AT89LP4052	4K		256	2	2	N	Y	Y	Y	N	20	Now
AT89LP428	4K	512	768	3	6	Y	Y	Y	2	N	28/32	Q1 2007
AT89LP828	8K	1K	768	3	6	Y	Y	Y	2	N	28/32	Q1 2007
AT89LP840	8K	512	768	3	6	Y	Y	Y	2	N	40/44	Q3 2007
AT89LP1640	16K	1K	768	3	6	Y	Y	Y	2	N	40/44	Q3 2007
AT89LP3240	32K	2K	1280	3	6	Y	Y	Y	2	10-bit	40/44	Q2 2007
AT89LP6440	64K	4K	2304	3	6	Y	Y	Y	2	10-bit	40/44	Q2 2007

Conclusion

The AT89LP family devices are cost-effective 8-bit microcontrollers ideal for applications requiring low power and high performance. These new microcontrollers reduce system cost with a variety of on-chip features enabling faster time-to-market. Ideal for Power Management, White Goods, and Universal Remote Control applications, the AT89LP family devices provide greater system-level integration. With the new AT89LP devices, system designers can enjoy up to 80% decrease in power consumption compared to classic 8051 microcontrollers at the same MIPS performance level. Consequently, the EMC characteristics also improve significantly.

Binary compatibility with the standard 8051-instruction set allows upward migration from multi-clock cycle 8051 cores to the higher performance AT89LP-series. Atmel's Single-Cycle AT89LP Flash Microcontrollers are easy to use, and offer a rich and powerful CISC instruction set at RISC performance.

References

1. Atmel 8051 datasheets and product documentation: www.atmel.com/products/8051

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